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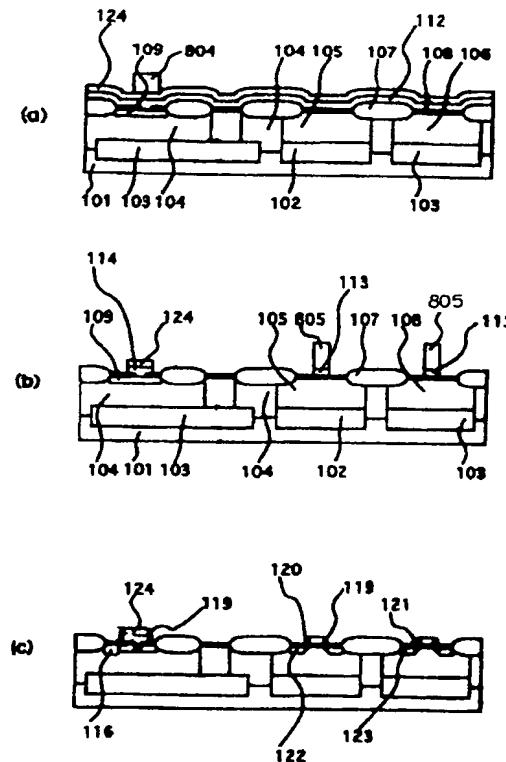
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### (54) A process for manufacturing a semiconductor device

(57) Implantation of a high concentration of P type impurity in an emitter electrode can be prevented during forming a source-drain of PMOS and a extrinsic base, by keeping an insulating film intact only on an emitter electrode and simultaneously patterning the insulating electrode and a gate electrode, leading to prevention of increase and dispersion of an emitter resistance.

FIG. 2



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**Description****BACKGROUND OF THE INVENTION****1. Field of the invention**

This invention relates to a process for manufacturing a semiconductor integrated circuit device comprising a bipolar transistor formed on a semiconductor substrate and a complementary field-effect transistor(hereinafter, referred to as CMOS).

**2. Description of the related art**

BiCMOS technology is one for forming a bipolar transistor having characteristics of high-speed actuation and high driving performance and a CMOS having a characteristic of low power consumption, on the same substrate, which is one of the most effective procedures for meeting recent demands on lower power consumption and higher speed in a semiconductor device.

Since BiCMOS technology requires many steps, cost reduction has been strongly desired. JP-A 4-74434 and JP-A 8-55924 have disclosed techniques for meeting such demands.

As the first prior art, description of JP-A 4-74434 will be briefly illustrated by referring to Figure 5(a) to (c) and Figure 6(a) to (c).

As seen in Fig. 5(a), on a P type silicon substrate 301 are formed an N<sup>+</sup> buried layer 303 and a P<sup>+</sup> buried layer 302; is grown an N type epitaxial layer 304; and then are formed an N well 305 and a P well 306.

Then, on the substrate are formed a field oxide film 307 by LOCOS technique and then a gate oxide film 308, and boron ion is implanted with a mask 901 to form a P type base area 309.

Then, as seen in Fig.5(b), an emitter contact 310 and a collector contact 311 are opened with a mask 902.

As seen in Fig.5(c), a polysilicon 302 is deposited over the whole surface, and then arsenic ion is implanted on a given area.

Then, as seen Fig.6(a), phosphorous ion is implanted in a given area with a mask 903.

Then, as seen Fig 6(b), the polysilicon 312 is selectively etched to form an emitter polysilicon 314, a collector polysilicon 315 and a gate polysilicon 313.

Herein, the arsenic ion is implanted for forming an emitter diffusion layer 317 which will be described later, while the phosphorous ion is implanted for forming a collector diffusion layer 318 and an N<sup>+</sup> type gate polysilicon 313 both of which will be described later.

Then, as seen in Fig.6(c), an N type LDD layer 320 and a P type LDD layer 321 are formed; an oxide film is deposited over the whole area of the wafer, and it was etched back by RIE technique to form a side wall 319 consisting of an oxide film.

Then, an N<sup>+</sup> type source-drain 322 is formed, and a

P<sup>+</sup> type source-drain 323 and a extrinsic base 316 are simultaneously formed.

Then, the substrate was treated by heat to form an emitter diffusion layer 317 and a collector diffusion layer 318, to give a device portion of a BiCMOS integrated circuit.

Next, as the second prior art, the technique described in JP-A 8-55924 will be briefly described by referring to Fig.7(a) to (c) and Fig 8(a) to (c).

As seen in Fig. 7(a), on a P type silicon substrate 401 are formed an N<sup>+</sup> buried layer 403, a P<sup>+</sup> buried layer 402, an N well 406 and a P well 405, and then boron ion is implanted through the first oxide film 404 about 30 nm thick, using a mask 911. The conditions of ion-implantation may be, for example,  $7.0 \times 10^{13} \text{ cm}^{-2}$  at 10 keV. Thus, a P type base area 409 is formed.

As seen in Fig.7(b), after removing the first oxide film 404, a gate oxide film(407) 10 nm thick is formed by thermal oxidation. Then, a part of the gate oxide film 408 for an emitter contact 410 is removed with a mask 912 by, for example, selectively etching with 10 % HF for 10 seconds.

Then, as seen in Fig.7(c), a polysilicon 412 about 350 nm thick is deposited over the whole area of the wafer by LPCVD technique, and then boron ion is implanted in an area where a gate of PMOS will be formed, with a mask 913, for example, under the conditions of  $2 \times 10^{15} \text{ cm}^{-2}$  at 20 keV.

Then, as seen in Fig.8(a), arsenic ion or phosphorous ion is implanted on the areas where an emitter and a gate of NMOS will be formed; for example, under the conditions of  $1 \times 10^{16} \text{ cm}^{-2}$  at 100 keV for arsenic.

Then, as seen Fig 8(b), the polysilicon 412 is selectively etched to form an emitter polysilicon electrode 414 and a gate polysilicon electrode 413.

Then, as seen in Fig.8(c), an N type LDD layer 420 and a P type LDD layer 421 are formed, and an dielectric film is deposited over the whole area of the wafer, and it was etched back to form a side wall 419 which consists of an oxide film, preferably of an oxide film and a nitride film on the oxide film.

Then, an N<sup>+</sup> type source-drain 422 is formed, and a P<sup>+</sup> type source-drain 423 and a extrinsic base 416 are simultaneously formed, and the substrate was treated by heat.

Herein, the gate of the PMOS is doped by an ion-implantation of a P<sup>+</sup> type source-drain 423, and the gate of the NMOS is doped by an ion-implantation of a N<sup>+</sup> type source-drain 422.

After above process, silicification may be conducted on the surfaces of the gate polysilicon electrode 413, the P<sup>+</sup> type source-drain 423, N<sup>+</sup> type source-drain 422 and/or the emitter polysilicon electrode 414 by a known technique.

**SUMMARY OF THE INVENTION**

Problems in the prior art in which a gate polysilicon

and an emitter polysilicon share a wiring, will be described by referring to Figure 9, wherein 501 is a P type silicon substrate, 502 is an N<sup>+</sup> type buried layer, 503 is an N type epitaxial layer, 504 is a collector diffusion layer, 505 is a field oxide film, 506 is an emitter polysilicon, 507 is a P type base area, 508 is an extrinsic base, 509 is a side wall and 916 is a mask.

In the prior art in which a gate polysilicon and an emitter polysilicon share a wiring layer, the N<sup>+</sup> type emitter polysilicon is separated from the P<sup>+</sup> type extrinsic base by a distance indicated by WEB in Fig.9(a). It provides a margin larger than an alignment deviation in an exposure step in a process for forming the extrinsic base. However, as scaling, i.e., size reduction and refinement, proceeds in a bipolar transistor, WEB becomes smaller as shown in Fig.9(b). Thus, when a deviation in alignment occurs in an exposure step in a process for forming the P<sup>+</sup> type extrinsic base, a mask 916 over the emitter polysilicon may be opened, for example, as shown in Fig.9(c), in which a high concentration of P type impurity may be implanted.

Such an event may cause deterioration in quality of a bipolar transistor such as;

- (1) increase of the emitter resistance of the bipolar transistor and increase of dispersion of the emitter resistance value, and
- (2) reduction in a current gain of the bipolar transistor and increase in dispersion of the current gain.

Thus, this invention is to provide a process for manufacturing a semiconductor device wherein the above deterioration in quality of a bipolar transistor can be prevented by avoiding implantation of a high concentration of P type impurity in an emitter polysilicon in a process for forming a extrinsic base of a bipolar transistor even when scaling proceeds in the bipolar transistor in which a wiring layer is shared by a gate polysilicon electrode and an emitter polysilicon electrode.

To solve the above problems, this invention provides a process for manufacturing a semiconductor device, comprising forming a gate oxide film and opening an emitter contact on the surface of a semiconductor substrate; forming a conducting film and an insulating film on the gate oxide film; selectively keeping the insulating film intact on an area including the area for the emitter contact; forming a mask for a gate electrode; and simultaneously forming a gate electrode and an emitter electrode.

Furthermore, this invention provide a process for manufacturing a semiconductor device, comprising forming a gate oxide film and opening an emitter contact on the surface of a semiconductor substrate; forming a conducting film and an insulating film on the gate oxide film; selectively keeping the insulating film intact on an area including the area for the emitter contact; forming a mask for a gate electrode and an emitter electrode; and simultaneously forming a gate electrode and an emitter

electrode.

According to the process for manufacturing a semiconductor device of this invention, an insulating film is pre-formed on an area for forming an emitter polysilicon, and then, in a process for forming a gate polysilicon and an emitter polysilicon the emitter polysilicon and the gate polysilicon are etched, employing, as a mask during etching, an insulating film or a combination of an insulating film and a photoresist for the former, and a photoresist for the latter. Thus, the insulating film can be kept intact at least on the area in which ion may be implanted during a process for forming a extrinsic base, and the insulating film acts as a mask for ion-implantation during the process for forming a P<sup>+</sup> type extrinsic base to prevent implantation of a high concentration of P type impurity in an emitter polysilicon.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a sectional process drawing to illustrate Example 1 according to this invention.

Figure 2 shows another sectional process drawing to illustrate Example 1 according to this invention.

Figure 3 shows a sectional process drawing to illustrate Example 2 according to this invention.

Figure 4 shows another sectional process drawing to illustrate Example 2 according to this invention.

Figure 5 shows a sectional process drawing to illustrate the first prior art.

Figure 6 shows another sectional process drawing to illustrate the first prior art.

Figure 7 shows a sectional process drawing to illustrate the second prior art.

Figure 8 shows another sectional process drawing to illustrate the second prior art.

Figure 9 shows sectional views to illustrate the problems of the prior art.

Figure 10 shows top and sectional views to illustrate the problems in Example 1 according to this invention.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

##### Example 1

An embodiment of this invention will be described by referring to Fig.1(a) to (c) and Fig.2(a) to (c).

As shown in Fig.1(a), in accordance with the prior art, on a P type silicon substrate 101 are formed a N<sup>+</sup> buried layer 103 and a P<sup>+</sup> buried layer 102; is grown a N type epitaxial layer 104; and are further formed a N well 106 and a P well 105. Then, a field oxide film 107 from 200 to 500 nm thick is formed by a known technique; a gate oxide film 108 from 3 to 10 nm thick is formed by thermal oxidation; and boron ion is implanted using a mask 801 of, for example, a photoresist, to form a P type base area 109.

Then, as seen in Fig.1(b), a part of the gate oxide film 108 on an emitter contact 110 is selectively removed using a mask 802 of, for example, photoresist by, for example, wet etching or dry etching.

Then, as seen in Fig.1(c), a polysilicon 112 from 100 to 500 nm thick is grown over the whole surface of the wafer, wherein the polysilicon is preferably non-doped or grown containing an N type impurity such as phosphorous and arsenic in concentration of  $1 \times 10^{17}$  to  $1 \times 10^{21} \text{ cm}^{-3}$ , preferably  $1 \times 10^{18}$  to  $1 \times 10^{20} \text{ cm}^{-3}$ , by employing a known CVD technique.

After growing of the polysilicon, the area including a region for forming an emitter polysilicon is opened using a mask 803 of, for example, photoresist; for example, an N<sup>+</sup> type impurity such as phosphorous and arsenic ion is implanted at, e.g., 5 to 70 keV to achieve its total concentration of  $1 \times 10^{19}$  to  $1 \times 10^{21} \text{ cm}^{-3}$  in the polysilicon.

The above ion-implantation is not necessary when the polysilicon is grown containing the impurity in a high concentration in the above step of growing the polysilicon. ,

Then, as seen in Fig.2(a), a silicon oxide film from 100 to 300 nm thick and the first insulating film 124 such as a silicon nitride film are grown by, for a known process such as a CVD technique, and then a mask 804 of, for example, photoresist is formed on the area for forming an emitter polysilicon.

Then, as seen in Fig.2(b), the first insulating film 124 is subject to patterning by a known anisotropic etching technique, the mask 804 is removed, a mask 805 of, for example, photoresist is formed for forming a gate polysilicon, and then the polysilicon is selectively etched by a known technique.

During the process, the first insulating film 124 on the emitter polysilicon and a mask 805 on the gate polysilicon play a role of a mask to the above etching.

Then, as seen in Fig.2(c), a N type LDD layer 120 and a P type LDD layer 121 are formed by a known technique; an insulating film such as a silicon oxide film and a silicon nitride film 30 to 200 nm thick is grown over the whole surface by a known process such as a CVD technique; it is etched back by a known anisotropic etching to form a side wall 119; a N<sup>+</sup> type source-drain 122 is formed; a P<sup>+</sup> type source-drain 123 and a extrinsic base 116 are simultaneously formed; and finally the substrate is treated by heat.

During formation of the extrinsic base 116, a high concentration of P type impurity is not implanted to the emitter polysilicon since the emitter polysilicon is completely covered with the first insulating film 124.

Furthermore, after completion of the above procedure, silicification may be conducted on the surfaces of the gate polysilicon 113, the P<sup>+</sup> type source-drain 123, the N<sup>+</sup> type source-drain 122 and/or the extrinsic base 116 by a known technique as is in the second prior art, which is not shown in the drawings. During the process, the emitter polysilicon is not silicified since it is completely covered with the first insulating film 124.

Next, further scaling will be described by referring to Fig.10(a) and (b), wherein 601 is a field oxide film; 602 is a base diffusion layer; 603 is a collector diffusion layer; 604 is an emitter contact; 605 is an emitter polysilicon; 606 is an interlayer insulating film, 607 is a contact, 608 is a contact plug; and 609 is a metal line.

In the above Example 1, the first insulating film 124 completely covers over the emitter polysilicon 114 as shown in Fig.2(c); the structure is as shown in the top and the sectional views of Fig.10(a).

In general, the base diffusion layer width 610 in Fig.10(a) should be subject to scaling for further improving performance and speed of the bipolar transistor.

For scaling of the base diffusion layer width 610 of the bipolar transistor, the linewidth and the line pitch of the metal line 609 should be reduced at the same time. However, since an electric current as high as several mA to several tens of mA is applied to emitter and collector electrodes in a bipolar transistor, reduction of the linewidth of the metal line 609 may cause deterioration of resistance to electromigration and of the quality of the metal line. Therefore, a method for scaling without reduction of the linewidth of the metal line 609, is desired.

In the top view of Fig.10(b), scaling leads to a longer wire length for the emitter polysilicon 605 than one in Fig.10(a).

#### Example 2

Thus, it may be undesirable due to its causing increase of emitter resistance. As a specific procedure for solving the problem, the second embodiment according to this invention will be described.

The second embodiment of the process for manufacturing a semiconductor device according to the invention will be described by referring to Fig.3(a) to (c) and Fig.4.

Herein, the sectional views of Figs.3(b), 3(c) and 4 for the bipolar transistor are those taken on line E-F of Fig.3(a) for illustrating clearly.

In Figs.3 and 4, 201 is a P type silicon substrate; 202 is a P<sup>+</sup> type buried layer; 203 is a N<sup>+</sup> type buried layer; 204 is a N type epitaxial layer; 205 is a P well; 206 is a N well; 207 is a field oxide film; 208 is a gate oxide film; 209 is a P type base region; 213 is a polysilicon; 214 is an emitter polysilicon; 219 is a side wall; 220 is a N type LDD layer; 221 is a P type LDD layer; 222 is a N<sup>+</sup> type source-drain; 223 is a P<sup>+</sup> type source-drain; 224 is the second insulating film; 225 is a silicide layer; and 916 is a mask.

The sectional view for the semiconductor device according to Example 2 is as Fig.10(b).

The cross-sectional structure shown in Fig.1(c) is formed as described in Example 1. The following process will be described by referring to Fig.3. As shown in Fig.3(a), The second insulating film 224 from 100 to 300 nm thick is grown over the whole surface of the wafer by

a known process such as a CVD technique. The second insulating film 224 may be a silicon oxide film and a silicon nitride film. The insulating film 224 is formed in a manner that the film covers at least the area on the emitter polysilicon which may be implanted with a high concentration of P type impurity due to an alignment deviation during an exposure step in forming a extrinsic base of a bipolar transistor.

Then, as seen in Fig.3(b), a mask 806 of, for example, photoresist is formed for forming a gate electrode and a withdrawal part of the emitter polysilicon. An emitter polysilicon 214 and a gate polysilicon 213 are formed by a known anisotropic polysilicon etching, using, as a mask for etching, the insulating film 224 and the mask 806 for the former and the mask 806 for the latter.

Then, as seen in Fig.3(c), a N type LDD layer 220 and a P type LDD layer 221 are formed by a known technique; an insulating film such as a silicon oxide film and a silicon nitride film 30 to 200 nm thick is grown over the whole surface by a known process such as a CVD technique; and it is etched back by a known anisotropic etching to form a side wall 219.

Then, as shown in Fig.4, a N<sup>+</sup> type source-drain 222 is formed; a P+ type source-drain 223 and a extrinsic base 216 are simultaneously formed; and the substrate is treated by heat.

Since the second insulating film 224 covers at least the area on the emitter polysilicon which may be implanted with a high concentration of P type impurity during formation of the P<sup>+</sup> type source-drain 223 and the extrinsic base 216, the area is not implanted with a high concentration of P type impurity. During the process, the gate of PMOS is subject to doping, on which a final concentration of impurity depends.

The gate of NMOS is subject to doping during implantation of the N<sup>+</sup> type source-drain 222, on which a final concentration of impurity depends.

Furthermore, silicification is conducted on the surfaces of the gate polysilicon 213, the P<sup>+</sup> type source-drain 223, the N<sup>+</sup> type source-drain 222, the extrinsic base 216 and/or the withdrawal part of the emitter polysilicon 214 by a known technique as is in the second prior art, to form a silicide layer 225.

Since a part of the emitter polysilicon 605 has been silicified to have a sheet resistance of several to several tens of  $\Omega/\square$ , the resistance of the withdrawal can be reduced, and thus the resistance of the emitter electrode, i.e., the emitter resistance, can be reduced.

As described above, according to the process of this invention for manufacturing a semiconductor device, deterioration in quality of a bipolar transistor can be prevented by avoiding implantation of a high concentration of P type impurity in an emitter polysilicon during a P<sup>+</sup> type extrinsic base formation step, to prevent;

(1) increase of the emitter resistance of the bipolar transistor and increase of dispersion of the emitter

resistance value, and

(2) reduction in a current gain of the bipolar transistor and increase in dispersion of the current gain.

5 Claims

- 10 1. A process for manufacturing a semiconductor device, comprising forming a gate oxide film and opening an emitter contact on the surface of a semiconductor substrate; forming a conducting film and an insulating film on the gate oxide film; selectively keeping the insulating film intact on an area including the area for the emitter contact; forming a mask for a gate electrode; and simultaneously forming a gate electrode and an emitter electrode.
- 15 2. A process for manufacturing a semiconductor device as is claimed in Claim 1, wherein the said conducting film is deposited in a form of non-doped polycrystal or amorphous silicon.
- 20 3. A process for manufacturing a semiconductor device as is claimed in Claim 1, wherein the said conducting film is polycrystal silicon deposited containing a N type impurity in concentration of  $1 \times 10^{17}$  to  $1 \times 10^{21} \text{ cm}^{-3}$ .
- 25 4. A process for manufacturing a semiconductor device as is claimed in Claim 1, wherein the said conducting film is a composite film consisting of a silicide with a high melting metal and polycrystal or amorphous silicon.
- 30 5. A process for manufacturing a semiconductor device as is claimed in Claim 1, wherein the said conducting film is a high-melting metal or a silicide with a high-melting metal.
- 35 6. A process for manufacturing a semiconductor device as is claimed in Claim 1, wherein the surfaces of the said gate electrode, the source-drain area and the extrinsic base of the bipolar transistor are silicified.
- 40 7. A process for manufacturing a semiconductor device, comprising forming a gate oxide film and opening an emitter contact on the surface of a semiconductor substrate; forming a conducting film and an insulating film on the gate oxide film; selectively keeping the insulating film intact on an area including the area for the emitter contact; forming a mask for a gate electrode and an emitter electrode; and simultaneously forming a gate electrode and an emitter electrode.
- 45 8. A process for manufacturing a semiconductor device as is claimed in Claim 7, wherein the said conducting film is deposited in a form of non-doped

polycrystal or amorphous silicon.

9. A process for manufacturing a semiconductor device as is claimed in Claim 7, wherein the said conducting film is polycrystal silicon deposited containing a N type impurity in concentration of  $1 \times 10^{17}$  to  $1 \times 10^{21} \text{ cm}^{-3}$ . 5
10. A process for manufacturing a semiconductor device as is claimed in Claim 7, wherein the said conducting film is a composite film consisting of a silicide with a high melting metal and polycrystal or amorphous silicon. 10
11. A process for manufacturing a semiconductor device as is claimed in Claim 7, wherein the said conducting film is a high-melting metal or a silicide with a high-melting metal. 15
12. A process for manufacturing a semiconductor device as is claimed in Claim 7, wherein the surfaces of the said gate electrode, the source-drain area, the extrinsic base of the bipolar transistor and the withdrawal part of the emitter electrode are silicified. 20 25

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F I G . 1

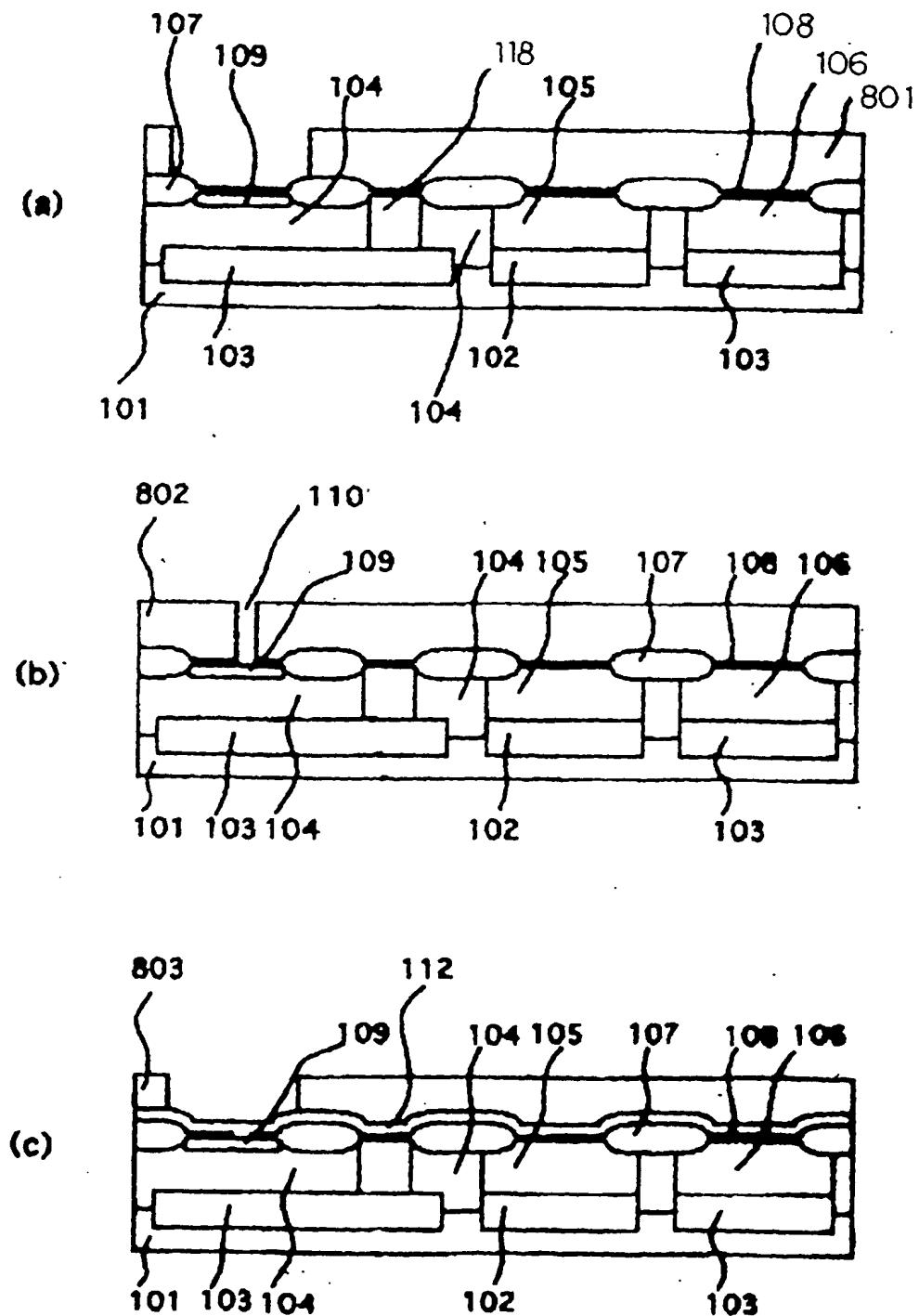


FIG. 2

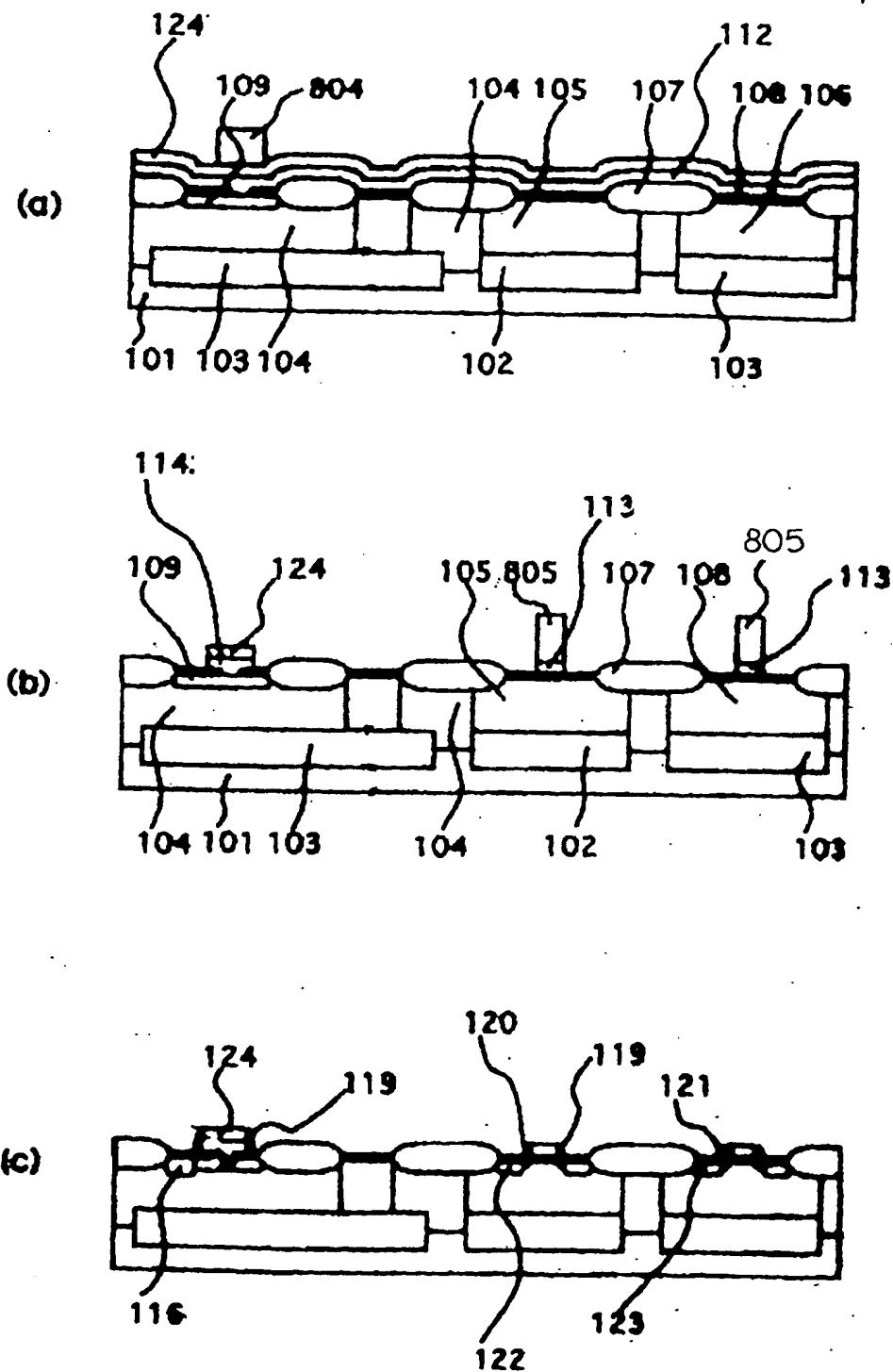
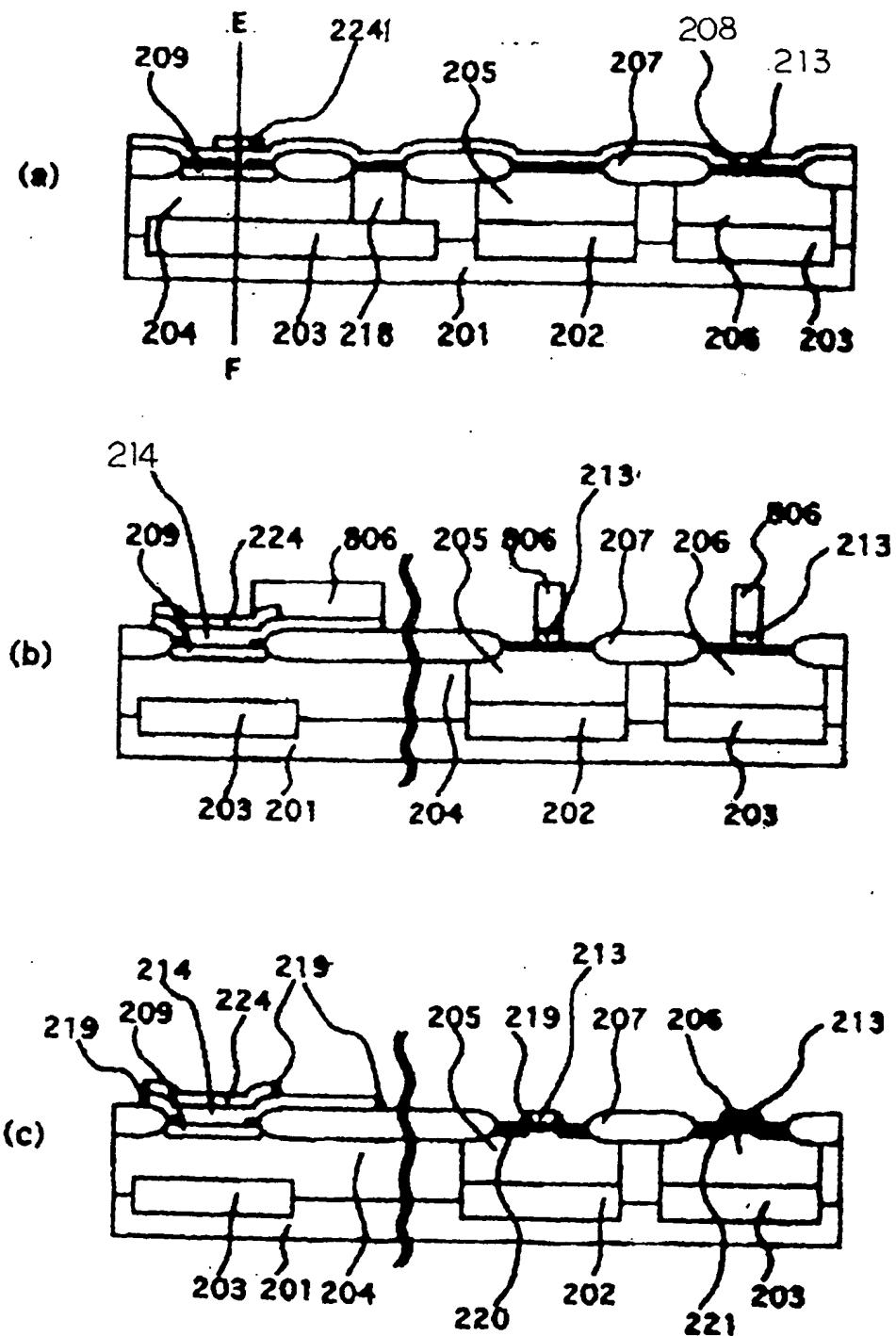
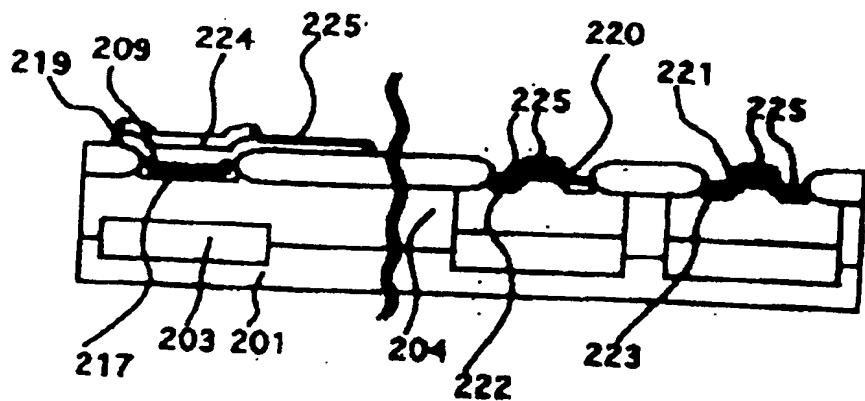


FIG. 3



F I G. 4



F I G . 5 ( P R I O R A R T )

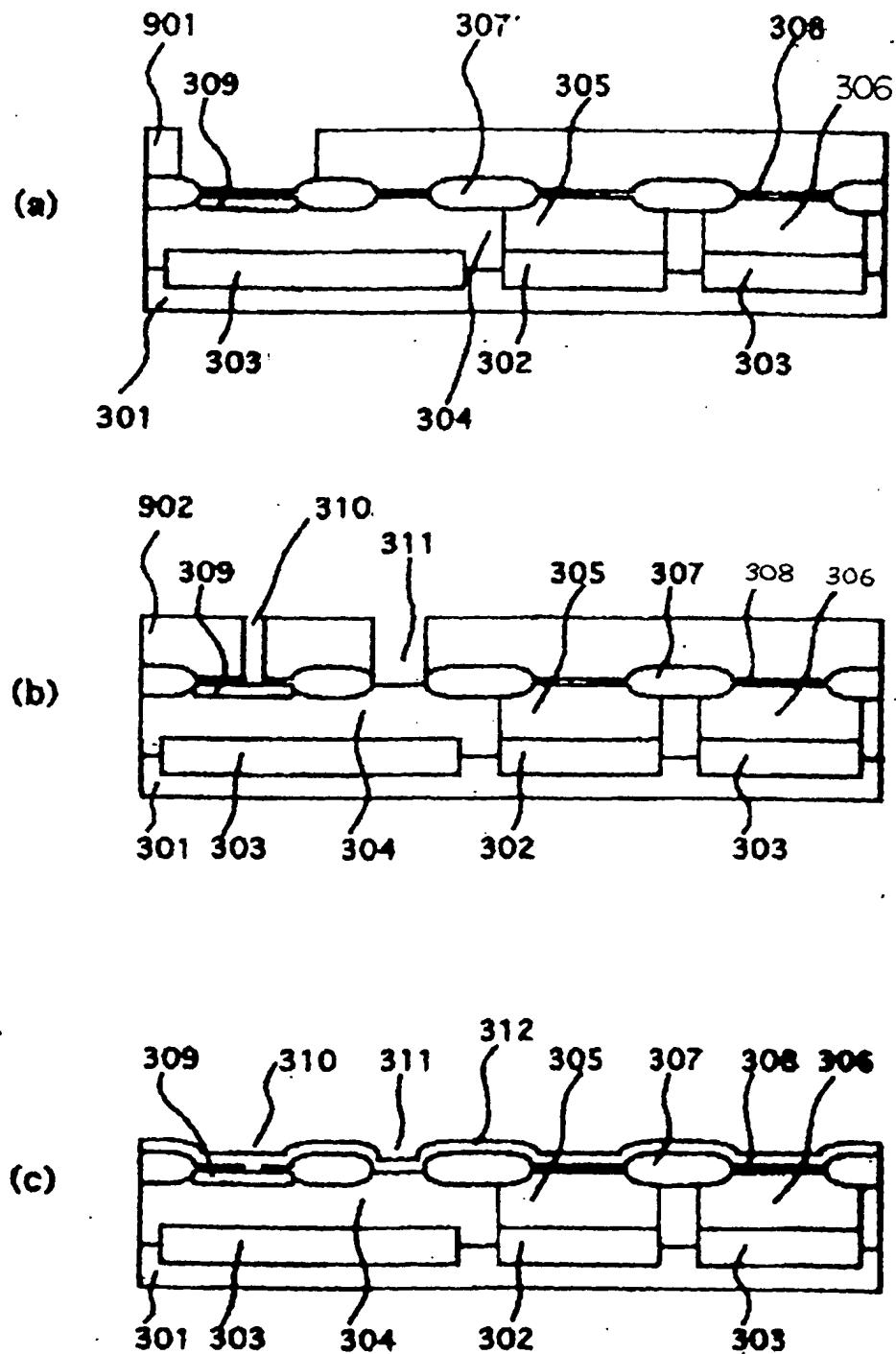


FIG. 6 (PRIOR ART)

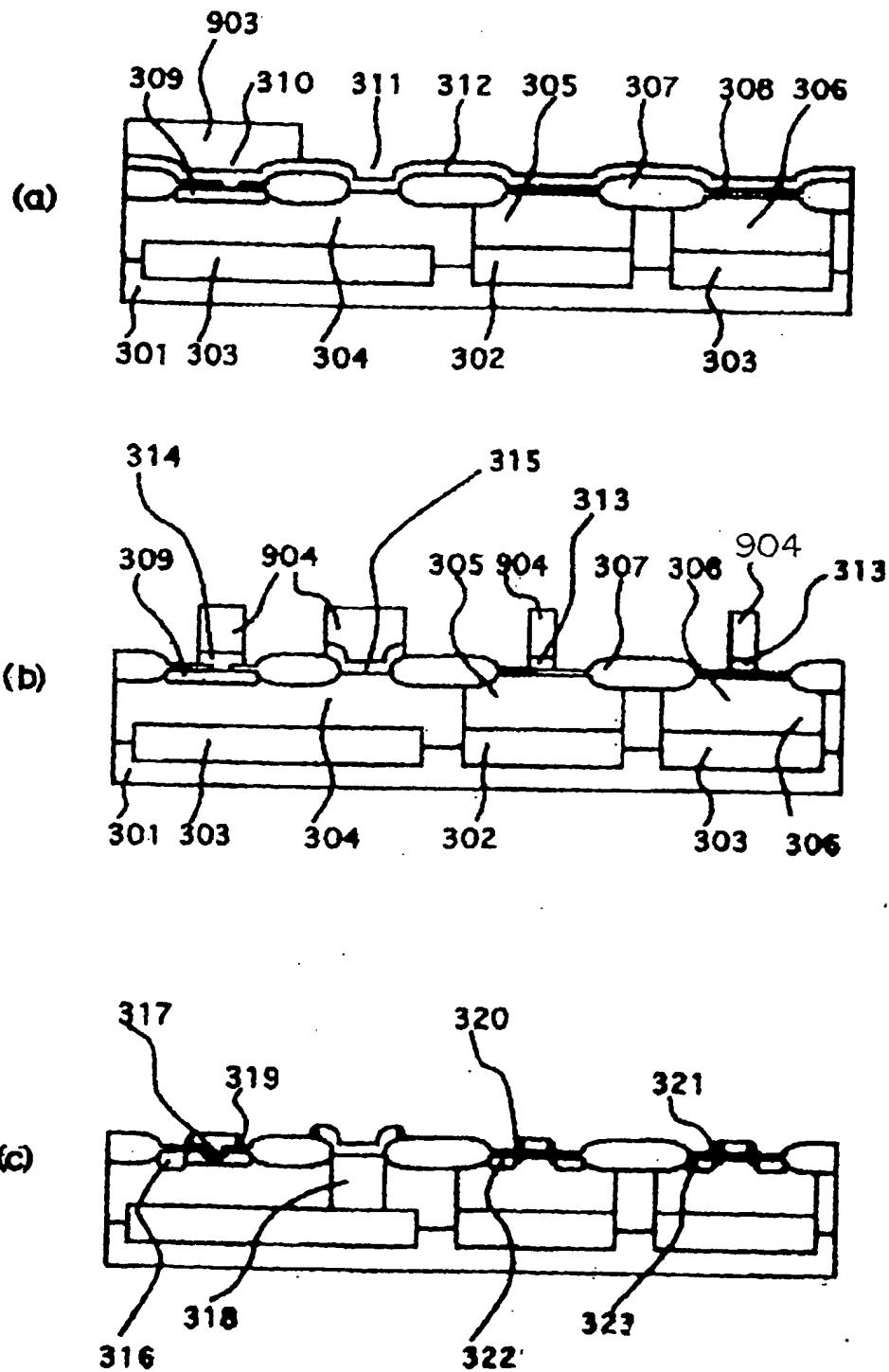


FIG. 7 (PRIOR ART)

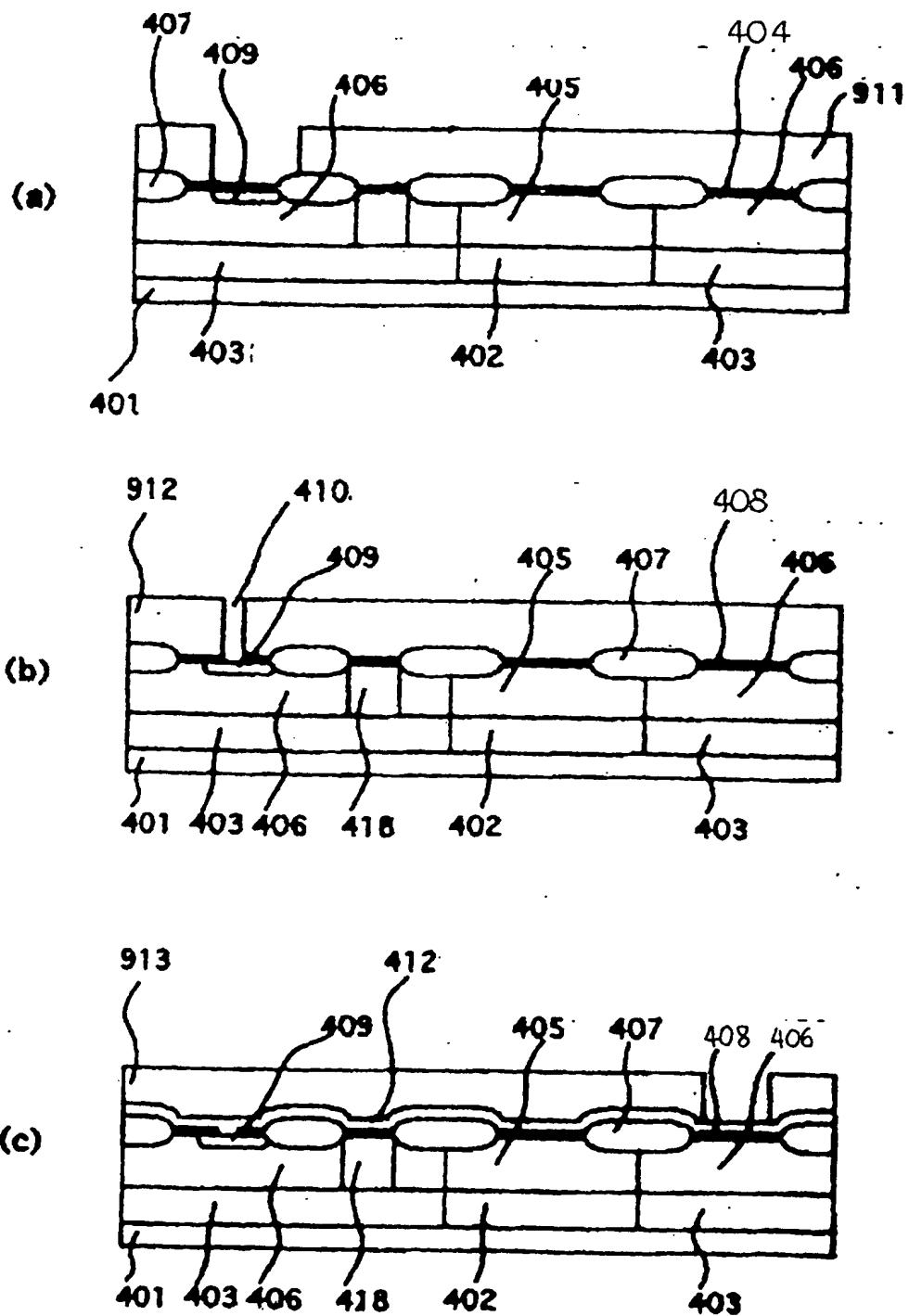
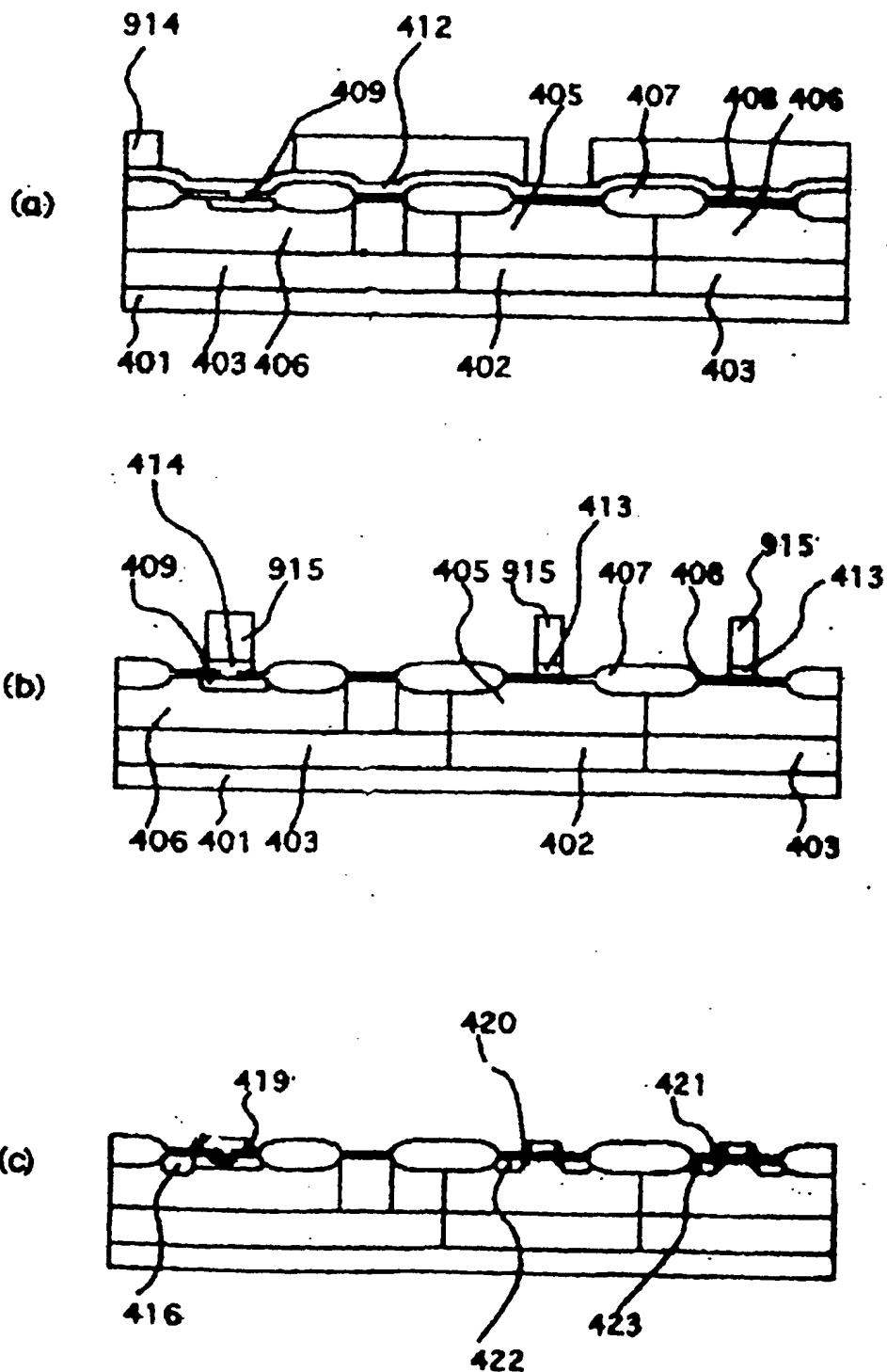


FIG. 8 (PRIOR ART)



F I G. 9 (P R I O R A R T)

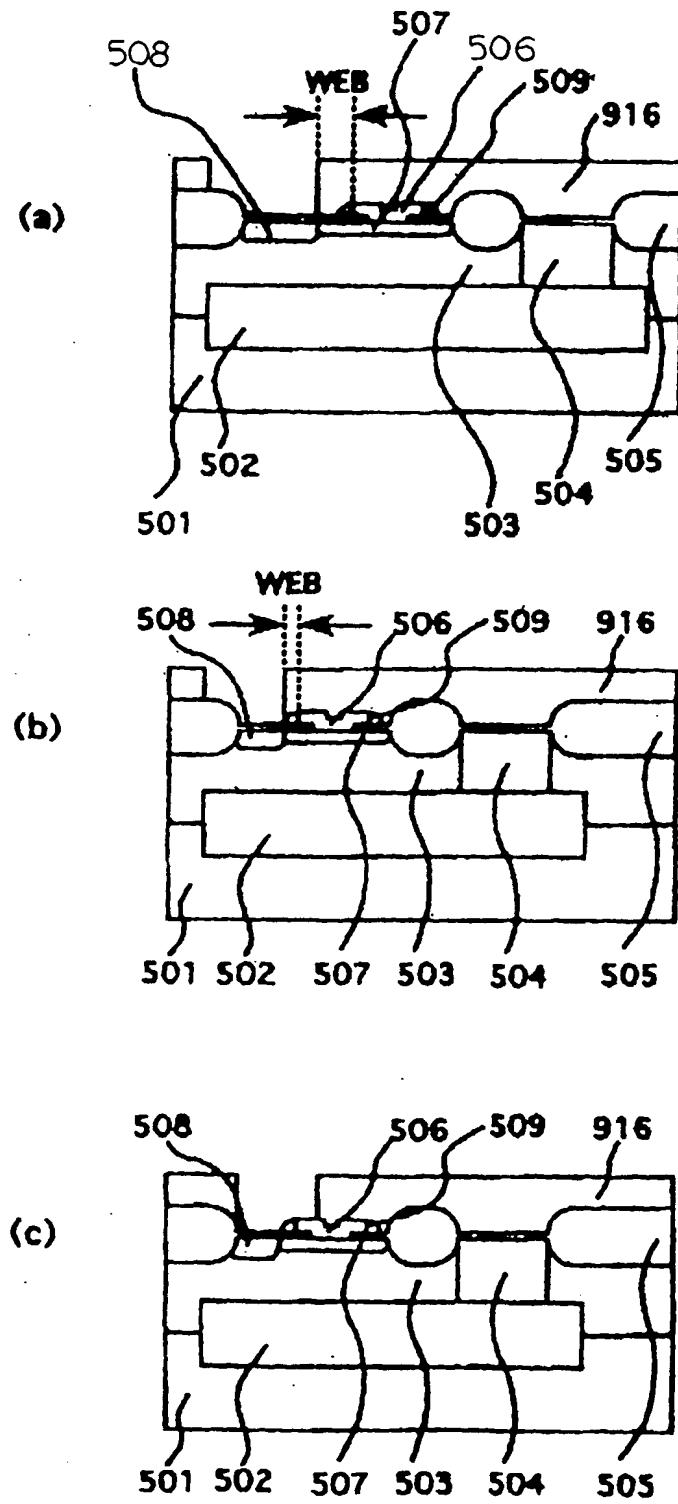
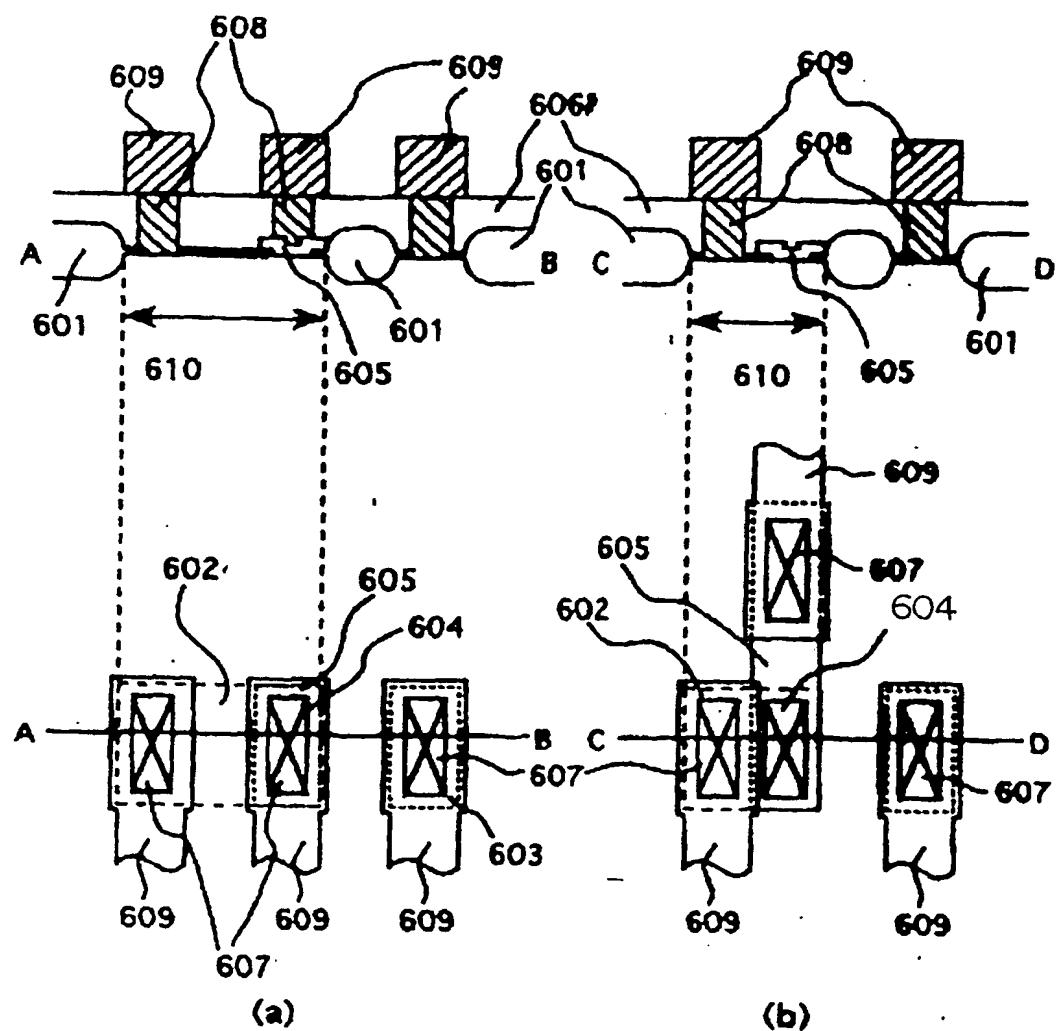


FIG. 10





European Patent  
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## EUROPEAN SEARCH REPORT

Application Number

EP 97 12 2190

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	US 5 089 429 A (HSU SHENG T)  * abstract; claims; figures * * column 1, line 35 - line 54 * * column 2, line 56 - column 3, line 14 * * column 3, line 66 - column 4, line 25 * -----	1,2,4,5, 7,8,10, 11	H01L21/8249
A	EP 0 244 171 A (BRITISH TELECOMM)  * abstract; claims; figures 1-8 * * column 1, line 35 - line 39 * * column 6, line 12 - line 21 * -----	1,2,4,5, 7,8,10, 11	
A	EP 0 694 963 A (TEXAS INSTRUMENTS INC)  * abstract; claims; figures * -----	1,2,4,5, 7,8,10, 11	
-----			
The present search report has been drawn up for all claims			
Place of search	Date of completion of the search		Examiner
THE HAGUE	31 March 1998		Wirner, C
CATEGORY OF CITED DOCUMENTS			
<input checked="" type="checkbox"/> particularly relevant if taken alone <input checked="" type="checkbox"/> particularly relevant if combined with another document of the same category <input type="checkbox"/> technological background <input type="checkbox"/> non-written disclosure <input type="checkbox"/> intermediate document			
T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			